REMARKS

This Amendment is submitted in response to the Examiner's Action mailed June 20, 2005, with a shortened statutory period of three months set to expire September 20, 2005. Claims 1-42 are currently pending. With this amendment, claims 1, 15, 29, and 33 have been amended.

Applicants have amended independent claims to describe specifying a particular level of lag. The particular level of lag is a specified synchronicity setting. A level of lag between computing entities is controlled by relaying commands until the synchronicity setting is reached. The relaying of additional commands is postponed after the synchronicity setting is reached. In this manner, the second computing entity lags behind the first computing entity by an amount of lag that is no greater than the specified synchronicity setting. Some examples of support for these amendments can be found in the specification on page 3, lines 3-12 and page 12, lines 15-28.

The Examiner rejected claims 1-7, 10-21, 24-31, 33-35, and 38-42 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,601,187 issued to *Sicola*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Applicants claim specifying a particular level of lag. The particular level of lag is a specified synchronicity setting. *Sicola* does not teach specifying a particular level of lag. *Sicola* acknowledges that lag may exist in an asynchronous copy situation; however, *Sicola* does not specify that lag.

The Examiner stated that *Sicola* teaches an amount of lag that is no greater than a specified synchronicity setting at column 11, lines 17-19. This section of *Sicola* teaches "when system 100 is in asynchronous mode, the remote site may lag behind by a bounded number of write I/O operations". Acknowledging that lag exists in an asynchronous mode is not the same as specifying a particular level of lag. *Sicola* does not teach specifying a particular level of lag. Therefore, *Sicola* does not anticipate Applicants' claims.

Applicants claim the specified level of lag being a specified synchronicity setting. Applicants also claim controlling a level of lag between computing entities by relaying commands until the synchronicity setting is reached. *Sicola* does not teach controlling a level of lag. As discussed above, *Sicola* merely acknowledges that lag may exist. *Sicola* does not

provide for controlling a level of lag. Because *Sicola* does not teach controlling a level of lag, *Sicola* does not anticipate Applicants' claims.

Further, *Sicola* does not teach controlling a level of lag by relaying commands until the synchronicity setting is reached. Nothing in *Sicola* teaches controlling lag by relaying commands until a synchronicity setting, which is the specified particular level of lag, is reached. Because *Sicola* does not teach controlling a level of lag by relaying commands until a synchronicity setting is reached, *Sicola* does not anticipate Applicants' claims.

Applicants claim postponing relaying additional commands after the synchronicity setting is reached, wherein the second computing entity lags behind the first computing entity by an amount of lag that is no greater than the specified synchronicity setting. *Sicola* does not teach postponing relaying additional commands after the synchronicity setting is reached. Therefore, *Sicola* does not anticipate Applicants' claims.

The remaining claims rejected as being anticipated by *Sicola* depend from independent claims that include the features discussed above. For the reasons given above, *Sicola* does not anticipate the remaining claims.

The Examiner rejected claims 8-9, 22-23, 32, and 36-37 under 35 U.S.C. § 103(a) as being unpatentable over *Sicola*. This rejection, as it might be applied to the claims as amended, is respectfully traversed.

Regarding claims 8, 9, and 32, the Examiner stated that *Sicola* teaches the amount of lag and the specified synchronicity setting being measured as amounts of data or number of devices. The Examiner takes Official Notice that there are well known ways of specifying lag such as through the use of buffers.

Sicola, however, does not teach specifying lag. *Sicola* states that lag exists but does not teach a way of specifying the lag. *Sicola* does not teach controlling a level of lag. *Sicola* does not teach controlling lag by relaying commands until the synchronicity setting is reached. *Sicola* does not teach postponing relaying additional commands after the synchronicity setting is reached. Therefore, the combination of *Sicola* with the use of buffers does not render Applicants' claims unpatentable.

Regarding claims 22-23, the Examiner stated that *Sicola* teaches a computer program product. *Sicola*, however, does not teach specifying lag. *Sicola* states that lag exists but does not teach a way of specifying the lag. *Sicola* does not teach controlling a level of lag. *Sicola* does

not teach controlling lag by relaying commands until the synchronicity setting is reached. *Sicola* does not teach postponing relaying additional commands after the synchronicity setting is reached. Therefore, *Sicola* does not render Applicants' claims unpatentable.

Regarding claims 36-37, the Examiner stated that *Sicola* teaches a processing unit, memory, and set of instructions. *Sicola*, however, does not teach specifying lag. *Sicola* states that lag exists but does not teach a way of specifying the lag. *Sicola* does not teach controlling a level of lag. *Sicola* does not teach controlling lag by relaying commands until the synchronicity setting is reached. *Sicola* does not teach postponing relaying additional commands after the synchronicity setting is reached. Therefore, *Sicola* does not render Applicants' claims unpatentable.

Sicola does not describe, teach, or suggest specifying a particular level of lag, the particular level of lag being a specified synchronicity setting, a level of lag between computing entities being controlled by relaying commands until the synchronicity setting is reached, or the relaying of additional commands being postponed after the synchronicity setting is reached. Therefore, *Sicola* does not anticipate Applicants' claims or render them unpatentable.

Applicants believe the application is in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 09.20.05

Respectfully submitted,

Lisa Yociss

Lisa L.B. Yociss
Reg. No. 36,975
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants